Listing of Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Previously Presented) A trace buffer circuit comprising:

a plurality of interconnected registers, including a first end register to input and output addresses of fetched instructions during a trace operation, a second end register, and a plurality of middle registers connected between said first end register and said second end register;

a write path to shift an instruction address in one of said plurality of interconnected registers by two registers toward the second end register on a write operation;

a first holding register;

a second holding register;

a first comparator to compare a new branch target address corresponding to a loop in the first holding register to a stored branch target address in the first end register;

a second comparator to compare a new branch source address corresponding to the loop in the second holding register to a stored branch source address in a first adjacent register, said

first adjacent register being connected to the first end register on a read path; and

a compression indication circuit to generate a compression indicator in response to the new branch target address matching the stored branch target address and the new branch source address matching the stored branch source address.

2. (Original) The circuit of claim 1, further comprising:

a read path to shift the instruction address by one register toward the first end register on a read operation.

3. (Previously Presented) The circuit of claim 1, wherein the trace buffer operates as a first-in first-out (FIFO) register on the write operation and a last-in first-out (LIFO) register on the read operation.

4. (Original) The circuit of claim 1, wherein the instruction address comprises a 32-bit word.

5. (Original) The circuit of claim 4, wherein each of the first and second end registers and the plurality of interconnected registers comprise a 32-bit register.

6. (Original) The circuit of claim 5, wherein the plurality of interconnected registers comprise thirty-two registers.

7. (Original) The circuit of claim 5, further comprising:

a 64-bit write bus to write a 64-bit address pair to the first end register and an adjacent register on the write operation; and

a 32-bit read bus to read a 32-bit instruction address from the first end register on the read operation.

8. (Canceled)

9. (Previously Presented) The circuit of claim 1, wherein the compression indication circuit operates to set a least significant bit of the stored branch target address in response to the new branch target address matching the stored branch target address and the new branch source address matching the stored branch source address.

10. (Previously Presented) The circuit of claim 1, further comprising:

a second adjacent register in said plurality of registers, said second adjacent register being connected to the first adjacent register on the read path;

a third adjacent register in said plurality of registers, said third adjacent register being connected to the second adjacent register on the read path;

a third comparator to compare the new branch target address in the first holding register to a second stored branch target address in the second adjacent register; and

a fourth comparator to compare the new branch source address in the second holding register to a second stored branch source address in the third adjacent register,

wherein the compression indication circuit operates to generate a compression indicator in response to the new branch target address matching the second stored branch target address in the second adjacent register and the new branch source address matching the second stored branch source address in the third adjacent register.

11. (Original) The circuit of claim 10, wherein the compression indication circuit operates to set a least significant bit of the stored branch source address in the third adjacent register in response to the new branch target address matching the stored branch target address in the second adjacent register and the new branch source address matching the stored branch source address in the third adjacent register.

12. (Original) The circuit of claim 1, further comprising a valid bit buffer comprising:

a first end flip-flop to input and output valid bits from the valid bit buffer;

a second end flip-flop;

a plurality of interconnected flip-flops connected between said first end flip-flop and said second end flip-flop;

a write path to shift a valid bit in one of said plurality of interconnected flip-flops by two flip-flops to a downstream flip-flop on a write operation; and

a read path to shift the valid bit by one flip-flop toward an upstream flip-flop on a read operation.

13. (Previously Presented) A pipelined processor comprising:

a trace buffer circuit connected to the pipelined digital signal processor, said trace buffer circuit comprising:

a plurality of interconnected registers, including a first end register to input and output addresses of fetched instructions during a trace operation, a second end register, and a plurality of middle registers connected between said first end register and said second end register;

a write path to shift an instruction address in one of said plurality of interconnected registers by two registers toward the second end register on a write operation; and

a read path to shift the instruction address by one register toward the first end register on a read operation.

14. (Original) The processor of claim 13, wherein the trace buffer operates as a first-in first-out (FIFO) register on the write operation and a last-in first-out (LIFO) register on the read operation.

15. (Original) The processor of claim 13, wherein the instruction address comprises a 32-bit word.

16. (Original) The processor of claim 15, wherein each of the first and second end registers and the plurality of interconnected registers comprise a 32-bit register.

17. (Original) The processor of claim 16, further comprising:

a 64-bit write bus to write a 64-bit address pair to the first end register and an adjacent register on the write operation; and

a 32-bit read bus to read a 32-bit instruction address from the end first register on the read operation.

18. (Previously Presented) A method comprising:

performing a trace operation including storing an address pair corresponding to a loop in fetched instructions in a trace buffer; and

performing a compression operation including

comparing the stored address pair to a new address pair in fetched instructions, and

setting a least significant bit of an address in the stored address pair in response to the new address pair matching the stored address pair.

19. (Original) The method of claim 18, further comprising:

discarding the new address pair in response to the new address pair matching the stored address pair.

20. (Original) The method of claim 18, further comprising:

storing the stored address pair in a first pair of registers; and

comparing the new address pair to the stored address pair.

21. (Original) The method of claim 20, further comprising:

writing the new address pair to the first pair of registers in response to the new address pair not matching the stored pair.

22. (Previously Presented) The method of claim 20, further comprising:

comparing the new address pair to a second stored address pair in a second pair of registers adjacent the first pair of registers;

setting a least significant bit of an address in the second stored address pair in response to the new address pair matching the second stored pair; and

writing the new address pair to the first pair of registers in response to the new address pair not matching the second stored pair.

23. (Original) The method of claim 22, further comprising:

discarding the new address pair in response to the new address pair matching the second stored address pair.

Claims 24-26. (Canceled)

27. (Previously Presented) An apparatus, including instructions residing on a machine-readable medium, for use in a trace buffer, the instructions operable to cause a machine to:

perform a trace operation including storing an address pair corresponding to a loop in fetched instructions in the trace buffer; and

perform a compression operation including

comparing the stored address pair to a new address pair in fetched instructions, and

setting a least significant bit of an address in the stored address pair in response to the new address pair matching the stored address pair.

28. (Original) The apparatus of claim 27, further comprising instructions causing the machine to:

discard the new address pair in response to the new address pair matching the stored address pair.

29. (Original) The apparatus of claim 27, further comprising instructions causing the machine to:

store the stored address pair in a first pair of registers; and

compare a new address pair to a stored address pair in the first pair of registers.

30. (Original) The apparatus of claim 29, further comprising instructions causing the machine to:

write the new address pair to the first pair of registers in response to the new address pair not matching the stored pair.

31. (Previously Presented) The apparatus of claim 29, further comprising instructions causing the machine to:

compare the new address pair to a second stored address pair in a second pair of registers adjacent the first pair of registers;

set a least significant bit of an address in the second stored address pair in response to the new address pair matching the second stored pair; and

write the new address pair to the first pair of registers in response to the new address pair not matching the second stored pair.

32. (Original) The apparatus of claim 31, further comprising instructions causing the machine to:

discard the new address pair in response to the new address pair matching the second stored address pair.

33. (Previously Presented) The method of claim 18, wherein said address in the address pair comprises a branch target address.

34. (Previously Presented) The method of claim 22, wherein said address in the second address pair comprises a branch source address.